

# PATENT ABSTRACTS OF JAPAN

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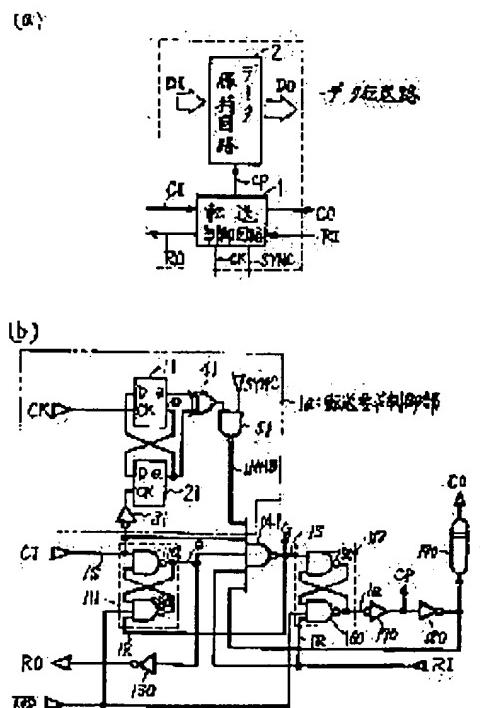
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## (54) SELF-SYNCHRONOUS TRANSFER CONTROL CIRCUIT

(57) Abstract:

PURPOSE: To provide a self-synchronous transfer control circuit having a function capable of suppressing or permitting transfer operation at optional required timing.

CONSTITUTION: Each data transmission line includes a self-synchronous transfer control circuit 1 and a data holding circuit 2 for latching input data DI in accordance with a pulse input from a pulse output terminal CP of the circuit 1 and sending output data DO to the succeeding transmission line. The circuit 1 includes further transfer request control part 1a, which sets up the circuit 1 to a permission mode or a suppressing mode for conventional self-synchronous transfer control operation based upon a mode signal applied from the external to its mode input terminal SYSN. In the suppressing mode, a transfer request signal applied to a pulse input terminal CI of the circuit 1 is controlled so as to be transmitted to the succeeding transfer control circuit in accordance with a clock applied from the external to the terminal CK of the control part 1a.



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